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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,883	02/19/2002	Raymond John Balzer	10010880-1	6255

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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,883	BALZER, RAYMOND JOHN	
	Examiner	Art Unit	
	John P. Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005 and 22 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-52* is/are rejected.

7)☒ Claim(s) *44-52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's amendment of 6/15/2005 and RCE of 7/22/2005.

Claims 1-26 were canceled.

Claims 27-52 were added as new.

Claims 27-52 are pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/15/2005 has been entered.

Response to Amendment

2. In view of Claims 1-26 being canceled by the applicant, the examiner withdraws the rejections under 35 USC 103 of said claims.

3. New Claims 27-52 are prosecuted below.

Claim Objections

4. Claims 44-52 are objected to because of the following informalities: Each claim begins with, "The apparatus ...", but should instead recite, "The testing circuit ...". Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. Claim 43 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. The applicant claims "a first circuit" configured to provide a TMS input to a TAP controller, and "a second circuit" configured to change the state of the TAP controller when a ground bounce occurs. Neither of these circuits are supported in the Disclosure and therefore fail to comply with the written description requirement.

6. Claims 31 and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim limits "the at least three ... states" to four named states, and thus the claim is indefinite because the four named states are in conflict with the first requirement in the claim of three states.

Claim Rejections - 35 USC § 102

7. Claims 27, 32, 35, 36, 43, 45 and 49-52 are rejected under 35 U.S.C. 102(a) as being anticipated by the applicant's admitted prior art (herein AAPA) in the disclosure, pages 1- 10 and FIG.1-3.

As per Claim 27:

The AAPA teaches a method comprising: starting a boundary scan test (AAPA page 10 lines 3-5); transitioning a Test Access Port (TAP) controller when a ground bounce occurs during the boundary scan test (AAPA page 10 lines 6-17), the TAP controller being transitioned from any of at least three undetermined controller states (example in AAPA is UPDATE on page 10) to a determined controller state (RUN-TEST/IDLE as on page 10 of AAPA), whereby transitioning the TAP controller to a determined controller state (RUN-TEST/IDLE) recovers the TAP controller from the ground bounce during the boundary scan test (see AAPA page 10), and resuming the boundary scan test (AAPA page 10 lies 11-13) when the TAP controller has been recovered from the ground bounce.

As per Claim 32:

The AAPA further teaches the method recited in claim 27, wherein transitioning the TAP controller further comprises: providing a low Test Mode Select input to the TAP controller prior to a falling edge of a clock signal while in an UPDATE state (page 10 lines 6-8).

As per Claims 35 and 43:

The AAPA teaches an apparatus or a testing circuit for conducting a boundary scan test, the apparatus comprising: at least one Test Access Port (TAP) controller

(FIG.1 118); and means for transitioning the TAP controller (page 2 lines 12-20 provides the only means disclosed) when a ground bounce occurs during a boundary scan test (page 10), the transitioning means configured to transition the TAP controller from any of at least three undetermined controller states (example in AAPA is UPDATE on page 10) to a determined controller state (RUN-TEST/IDLE on page 10) to recover the TAP controller from the ground bounce (AAPA page 10 lines 6-17), thereby allowing the boundary scan test to resume when the TAP controller is recovered from the ground bounce (AAPA page 10 lies 11-13).

As per Claim 36:

The AAPA further teaches the apparatus recited in claim 35, wherein the transitioning means further comprises: means for providing the TAP controller with a low Test Mode Select input prior to a falling edge of a clock signal while in an update state (same means as in Claim 35 plus page 10 lines 6-8).

As per Claim 45:

The AAPA further teaches the apparatus recited in claim 43, wherein the TAP controller is one of a plurality of controllers in a boundary scan chain (FIG.1 118 and FIG.2).

As per Claim 49:

The AAPA further teaches the apparatus recited in claim 43, wherein the second circuit is further configured to operationally transition the TAP controller from an undetermined data state to a determined data state (page 10).

As per Claim 50:

The AAPA further teaches the apparatus recited in claim 49, wherein the TAP controller is one of a plurality of controllers in a boundary scan chain (AAPA FIG.2 and FIG.1 118).

As per Claim 51:

The AAPA further teaches the apparatus recited in claim 49, wherein the second circuit begins transitioning the TAP controller from the undetermined data state to the determined data state when the TAP controller has reached an UPDATE-DR state (example in AAPA is UPDATE on page 10).

As per Claim 52:

The AAPA further teaches the apparatus recited in claim 51, wherein the TAP controller is one of a plurality of controllers in a boundary scan chain (AAPA FIG.2 and FIG.1 118).

Claim Rejections - 35 USC § 103

8. Claims 28-31, 33, 34, 37-42, 44 and 46-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (herein AAPA) in the disclosure, pages 1- 10 and FIG.1-3, and further in view of Beausang et al. (herein Beausang), U.S. Patent No. 6012155.

As per Claim 28:

Where the AAPA fails, Beausang further teaches the method recited in claim 27, wherein the at least three undetermined controller states are selected from the group consisting of an UPDATE state, a RUN-TEST/IDLE state, a SELECT-DR-SCAN state,

and a CAPTURE-DR state. Beausang et al. does teach this feature in FIG.10 and beginning at column 9 line 23, ending at column 12 line 47, where the state transitions from any of the 16 states to the TEST-LOGIC-RESET state. And in column 2 lines 45-60, Beausang et al. cites advantages, one being the capability to verify the state of the TAP controller. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to include the process of Beausang et al., to recover to a known TAP state, with the ground bounce failure of the AAPA in order to provide better failure recovery.

As per Claims 29 and 31:

Beausang further discloses the method recited in claim 28, wherein the at least three undetermined controller states include an UPDATE state, a RUN-TEST/IDLE state, and a SELECT-DR-SCAN state. Beausang et al. does teach this feature in FIG.10 and beginning at column 9 line 23, ending at column 12 line 47, where the state transitions from any of the 16 states to the TEST-LOGIC-RESET state. And in view of the motivation previously stated, the claims are rejected.

As per Claim 30:

Beausang further discloses the method recited in claim 27, wherein the determined controller state is an UPDATE-DR state (see Table 2 for the sequences required to reach UPDATE-DR). And in view of the motivation previously stated, the claim is rejected.

As per Claim 33:

Where the AAPA fails, Beausang further discloses the method recited in claim 32, wherein transitioning the TAP controller further comprises: providing the TAP controller with a Test Mode Select input having the following bit pattern for a consecutive series of rising edges of clock signals: a plurality of lows, high, a plurality of lows, high, high (see Table 2 for sequence to BSD RUN-TEST/IDLE). And in view of the motivation previously stated, the claim is rejected.

As per Claim 34:

Where the AAPA fails, Beausang discloses the method recited in claim 32, wherein transitioning the TAP controller further comprises: providing the TAP controller with a Test Mode Select input having the following bit pattern for a consecutive series of rising edges of clock signals: low, high, low, high, high (see Table 2 for sequence to BSD UPDATE-DR). And in view of the motivation previously stated, the claim is rejected.

As per Claim 37:

Where the AAPA fails, Beausang discloses the apparatus recited in claim 36, wherein the determined controller state is an UPDATE-DR state. (see Table 2 for sequence to BSD UPDATE-DR). And in view of the motivation previously stated, the claim is rejected.

As per Claim 38:

Beausang further discloses the apparatus recited in claim 37, wherein the at least three undetermined controller states are selected from the group consisting of an UPDATE state, a RUN-TEST/IDLE state, a SELECT-DR-SCAN state, and a CAPTURE-

DR state (see Table 2 for the sequences required to reach UPDATE-DR). And in view of the motivation previously stated, the claim is rejected.

As per Claims 39 and 41:

Beausang further discloses the apparatus recited in claim 38, wherein the at least three undetermined controller states include an UPDATE state, a RUN-TEST/IDLE state, and SELECT-DR-SCAN state (see Table 2 for the sequences required to reach UPDATE-DR). And in view of the motivation previously stated, the claims are rejected.

As per Claim 40:

The AAPA further discloses the apparatus recited in claim 39, wherein the transitioning means further comprises: means for providing the TAP controller with a Test Mode Select input having the following bit pattern for consecutive series of rising edges of clock signals: low, high, low, high, high (page 2 lines 12-20 provides for teaching the only means disclosed). And in view of the motivation previously stated, the claims are rejected.

As per Claim 42:

The AAPA further teaches the apparatus recited in claim 41, wherein the transitioning means further comprises: means for providing the TAP controller with a Test Mode Select input having the following bit pattern for a consecutive series of rising edges of clock signals: a plurality of lows, high, a plurality of lows, high, high (teaching on page 2 lines 12-20 provides the only means disclosed). And in view of the motivation previously stated, the claims are rejected.

As per Claim 44:

Beausang further discloses the apparatus recited in claim 43, wherein the first circuit is further configured to provided the TAP controller with a Test Mode Select input having the following bit pattern for a consecutive series of rising edges of clock signals: a plurality of lows, high, a plurality of lows, high, high. (see Table 2 for sequence to BSD RUN-TEST/IDLE). And in view of the motivation previously stated, the claim is rejected.

As per Claim 46:

Beausang further discloses the apparatus recited in claim 43, wherein the at least four undetermined controller states include an UPDATE state, a RUN-TEST/DLE state, a SELECT-DR-SCAN state, and a CAPTURE-DR state (see Table 2 for the sequences required to reach UPDATE-DR). And in view of the motivation previously stated, the claim is rejected.

As per Claim 47:

Beausang further discloses the apparatus recited in claim 46, wherein the first circuit is further configured to provided the TAP controller with a Test Mode Select input having the following bit pattern for a consecutive series of rising edges of clock signals: a plurality of lows, high, a plurality of lows, high, high. (see Table 2 for sequence to BSD RUN-TEST/IDLE). And in view of the motivation previously stated, the claim is rejected.

As per Claim 48:

The AAPA further teaches the apparatus recited in claim 47, wherein the TAP controller is one of a plurality of controllers in a boundary scan chain (AAPA FIG.2 and FIG.1 118). And in view of the motivation previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

JOSEPH TORRES
PRIMARY EXAMINER